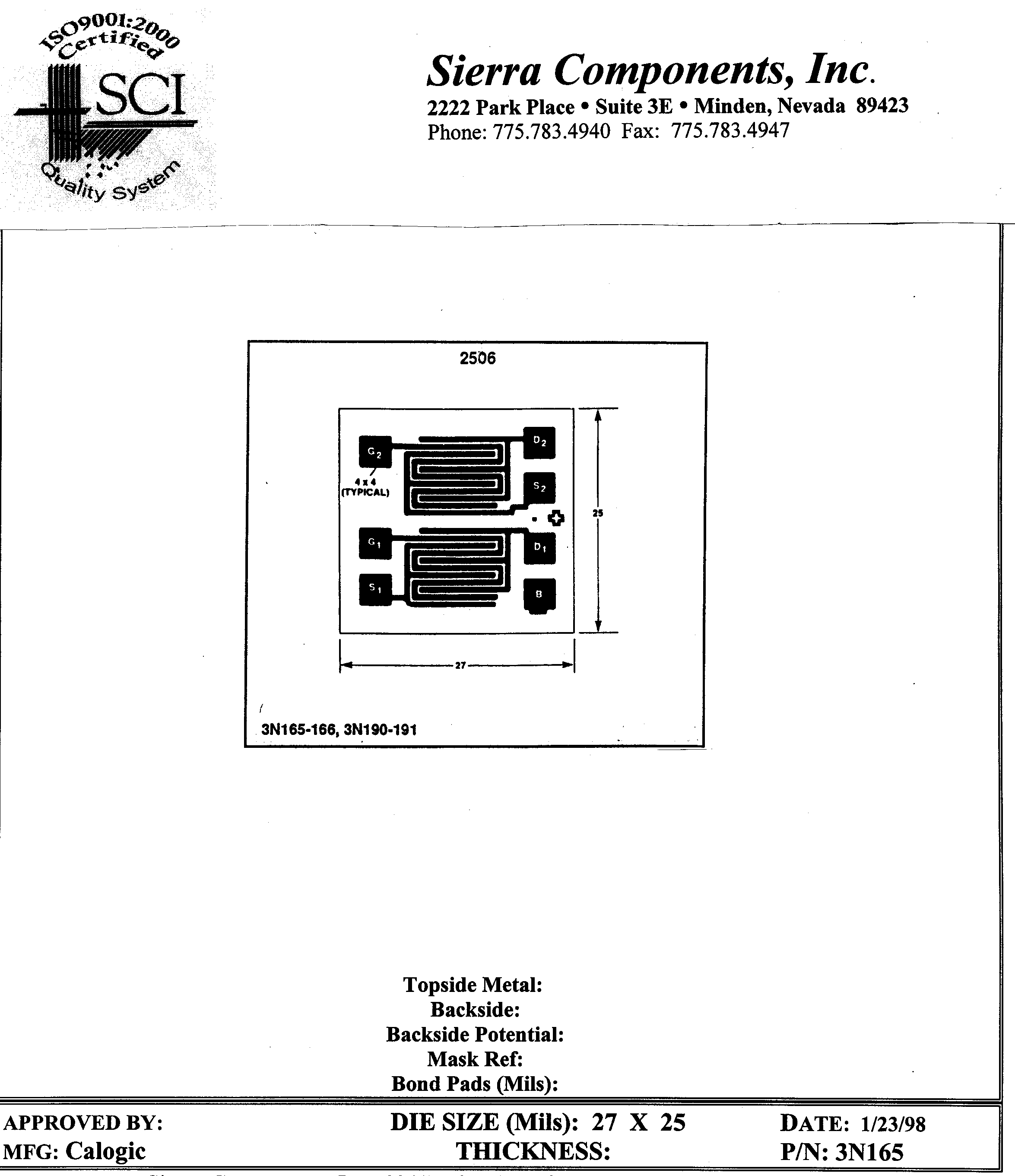
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.129”**

**PAD FUNCTION:**

1. **GND**
2. **INPUT +**
3. **INPUT +**
4. **V –**
5. **BAL**
6. **BAL/STROBE**
7. **OUTPUT V +**



**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” x .004” min.**

**Backside Potential:**

**Mask Ref: 2506**

**APPROVED BY: DK DIE SIZE .025” X .027” DATE: 12/15/22**

**MFG: CALOGIC THICKNESS .008” P/N: 3N165**

**DG 10.1.2**

#### Rev B, 7/19/02